

Serial No. 09/964,591

REMARKS

Claims 1-41 are pending and under consideration. Reconsideration is requested.

Items 3 and 5: Objection To Claims 1- 41 Because Of Informalities And Rejection Of Claims 1-41 Under 35 U.S.C. §112, first paragraph

In item 3, pages 2-8 of the Office Action, the Examiner objects to claims 1- 41 because of informalities. Using the objection of claim 1 as an example, the Examiner contends:

"a resource manager which manages said hardware resource data allocating a resource in which said resource manager allocates said hardware resource data meeting said request to said thread in accordance with a rule prescribed in advance" appears to be incorrect and it appears that it should be "a resource manager which manages said hardware resource."

(Action at page 2.)

In item 5, pages 8-16 of the Office Action, the Examiner rejects claims 1-41 under 35 U.S.C. §112, first paragraph contending the claims 1-41 contain subject matter that was not described in the specification. Using the rejection of claim 1 as an example, the Examiner contends:

there is no support for "making a request for hardware resource data relating to a hardware resource needed for execution of each of threads" and "dynamically allocating hardware resource data relating to necessary hardware resources" anywhere in the specification. This is new material added in the amendment (filed May 10, 2005) and not found in the original specification.

(Action at page 9.)

Applicants submit that the Examiner's contentions are not correct and that claims 1-41 are correct and properly supported as currently written. Applicants respectfully point out, for example, that as discussed in paragraph [0051]:

the resource 14 signifies information about a hardware resource. For example, each of processors, ASICs (Application Specific Integrated Circuits), operation units and other units is defined as resource data (emphasis added).

and in paragraph [0054]:

(t)he resource manager 12 manages resources 14 (type and number) needed for the progress of the threads 13 (the execution of the "methods"), and allocates a resource 14 corresponding to a resource request 19 to the request issuing thread 13 (emphasis added).

That is, the specification specifically discusses and provides the required support for claims 1-41, i.e., a resource manager that manages information about a hardware resource that is hardware resource data (resource 14).

Summary

Applicants submit that claims 1-41 comply 35 U.S.C. §112, first paragraph and request the objection and rejection by withdrawn.

Items 8-20: Rejection Of Claims 1-41 under 35 U.S.C. §103(a)

In items 8-20, pages 16-36 of the Office Action, the Examiner rejects claims 1-41 under 35 U.S.C. §103(a) as being unpatentable over Chen (U.S.P. 6,466,898) in view of combinations of Dearth et al. (U.S. P. 6,345,242), Dearth et al. (U.S.P. 5,812,824), Hollander (U.S.P. 6,347,388), Kinzelman et al. (U.S. P. 5,594,741), De Yong et al. (U.S.P. 5,355,435), Thekkath et al. (U.S.P. 6,490,642), Markov (U.S. P. 6,314,552), Kasuya (U.S.P. 6,077,304), Furuichi (U.S.P. 5,437,037), and Levy et al. (U.S.P. 6,092,175).

The rejections are traversed.

In items 21.1 -21.2, pages 37-38 of the Office Action, entitled Response To Arguments, the Examiner incorrectly contends:

applicants have introduced the term "hardware resource data" in this (previous) amendment. However, such a term was not used in the original application and hence is new material introduced, which is not allowed at this stage of prosecution.

The Examiner also incorrectly concludes that since Levy teaches a resource is dynamically allocated that:

there is no difference between what the applicants are claiming and what the Dearth et al. ('242), and Dearth et al. ('824) references teach for the simulation.

The Examiner bases this incorrect conclusion on the contention that "in any simulation, the real hardware will be assigned for executing the threads. The resource manager does not assign data but the resources," and that:

Dearth et al. ('242), and Dearth et al. ('824) references use distributed simulation assign the resources to multiple threads in distributed simulation. The resources allocated are real resources and not data.

(Action at page 37.)

Recited Features Not Taught By The Cited Art, Alone Or in Combination

Applicants submit that features recited by each of the independent claims, using claim 1 as an example, that a method of simulating an operation of a logical unit allocating hardware resource data relating to necessary hardware resources are not taught by the cited art, alone or in combination.

Further, Applicants submit that the Examiner's conclusion given his arguments is incorrect. Applicants submit that the Examiner appears to be contending that in essence:

1) since the cited references teach a resource manager manages hardware resources and does not assign data, that it is understood that by those skilled in the art that a resource manager manages hardware resources, and thus

Serial No. 09/964,591

2) claims 1-41 should be rejected.

However, Applicants submit that the conclusion the Examiner should properly have drawn, instead, is that that since features recited by the claims are not taught by the art, claims 1-41 distinguish over the art and should be allowed.

None of the cited art, alone or in combination teach a simulation using hardware resource data relating to necessary hardware resources as recited in each of the independent claims.

Levy does not teach a technique of a simulation of a logical unit but rather renaming of actual registers. The simulations taught by Dearth '242 and Dearth '824 do not teach allocation of data. Rather, Dearth '242 teaches (col. 5, starting at line 5):

each of tests 120A-C (FIG. 1), which is to carry out transactions with a simulated circuit, e.g., a circuit simulated by simulation systems 140A-C collectively, through a hub 130 is associated with a respective local synchronization thread ("LST") of hub 130. Each LST acts as a synchronization agent for a respective test and represents the synchronization state of the respective test.

Dearth '824 merely teaches (see, for example, col., 5, lines 5-10):

reserving of a device of a simulated circuit, the test prevents reservation of the device by other tests and can therefore interact with the device without interference with the interaction by another test.

For the convenience of the Examiner in distinguishing the present invention over the cited art, Applicants further points out to the Examiner the advantages according to an aspect of the present invention as recited by claims 1-41 have over the conventional art, for example, as discussed in paragraphs [0016]-[0017]:

an object of the invention to perform an operation simulation at an initial stage of a design of a logical unit for confirmation of a function and evaluation of an architecture, and further to cope flexibly with an alteration of the architecture, with a minimum of alteration of the description, thus considerably cutting down the design cost of the logical unit. . the resource manager executing the aforesaid steps 1) to 3) repeatedly in cooperation with each other until the execution of the thread reaches completion, for simulating an operation of the logical unit to be conducted up to the completion,

and paragraph [0027]:

a series of "functions" needed until the operation of the logical unit comes to completion are described by a plurality of sequential thread groups, or that they are represented by a plurality of sequential or concurrent thread groups. In the former case, the operation simulation becomes feasible in a state where the dependence among the "functions" of the logical unit is made clearer, while in the latter case, the operation simulation becomes possible with respect to a logical unit having a more complicated "function" configuration.

Such advantages are not realized by the cited art.

Applicants submit that since features recited by claims 1-41 are not taught by the cited art, the rejection should be withdrawn.

Examiner's Statement Without Support

Further, Applicants submit that the Examiner's statement that "in any simulation, the real hardware will be assigned for executing the threads" is without support, and that appropriate support should be provided or the rejections withdrawn.

The Applicants respectfully traverses the Examiner's statement and demands the Examiner produce authority for the statement. The Applicants specifically point out the following errors in the Examiner's action.

The noticed fact is not considered to be common knowledge or well-known in the art. In this case, the limitation is not of notorious character or capable of instant and unquestionable demonstration as being well-known. Instead, this limitation is unique to the present invention. See M.P.E.P. § 2144.03(A) ("the notice of facts beyond the record which may be taken by the Examiner must be "capable of such instant and unquestionable demonstration as to defy dispute").

Further, there is no evidence supporting the Examiner's assertion. See M.P.E.P. § 2144.03(B) ("there must be some form of evidence in the record to support an assertion of common knowledge").

In addition, it appears that the Examiner also bases the rejection, at least in part, on personal knowledge. The Examiner is required under 37 C.F.R. § 1.104(d)(2) to support such an assertion with an affidavit when called for by the Applicant. Thus, Applicantst call upon the Examiner to support such assertion with an affidavit.

Summary

Since features recited by claims 1-41 are not taught by the cited art and *prima facie* obviousness, is not established, the rejection should be withdrawn and the claims 1-41 allowed.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

MAY. 17. 2006 6:11PM

STAAS & HALSEY 202-434-1501

NO. 2182 P. 18/18

Serial No. 09/964,591

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

Date: May 17, 2006

By: Paul W. Bobowiec
Paul W. Bobowiec
Registration No. 47,431

1201 New York Avenue, NW, 7th Floor
Washington, D.C. 20005
Telephone: (202) 434-1500
Facsimile: (202) 434-1501

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being transmitted via facsimile to: Commissioner for Patents,
P.O. Box 1450 Alexandria, VA 22313-1450
on May 17, 2006

STAAS & HALSEY

By: Paul W. Bobowiec

Date: May 17, 2006